TES bolometer arrays for the QUBIC B-mode CMB experiment

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Abstract QUBIC is a ground-based experiment aiming to measure the B-mode polarization of the Cosmic Microwave Background (CMB). The developed instrument is an innovative two-frequency band bolometric interferometer that will operate at 300 mK with NbSi TES arrays. In this paper we describe the fabrication process of the detectors.

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Keywords Cryogenic detectors • Cosmic microwave background • Transition edge sensors

1 Introduction

Precise measurement of the light-polarization anisotropies in the Cosmic Microwave Background (CMB) is a big experimental challenge, requiring state of the art sensitive detectors, extended control of instrumental systematic effects and accurate subtraction of foregrounds emitted by the sky [1;2]. QUBIC is an experiment designed to observe the so-called B-modes of the CMB polarization with a setup able to control systematics with higher precision than usual imagers [3-5]. The instrument is a bolometric interferometer that will be deployed in 2020, at the Alto Chorrillos site in Argentina. It is equipped with two focal planes filtered at 150 GHz and 220 GHz and detectors based on time-domain SQUID multiplexed transition edge sensor (TES) arrays. The definition of a reproducible and robust microlithography fabrication process of the arrays was a high priority task for QUBIC, involving the CSNSM, C2N and APC laboratories.

2 Fabrication of the QUBIC detectors

The QUBIC focal planes consist of an assembly of 4 TES arrays forming a light sensitive surface of approximatively 100 mm diameter. Each array has 248 active pixels with a pitch of 3 mm and 8 test pixels placed on the side of the detection area. The active pixels are composed of a suspended meshed membrane with a NbSi TES on its center, and a light-absorption metallic grid. Several superconducting thin lines route the signals from the TES to a series of bonding-pads on the side of the array (Fig. 1). In the following we give a detailed description of the array fabrication process.

2.1 SOI substrates

The QUBIC arrays are manufactured using 3-inch diameter SOI (silicon on insulator) substrates. Wafer maximum dimension is limited by our e-beam evaporation bench for deposition of the NbSi TES thin films. The SOI substrates are double side polished and composed of three different layers whose thickness can be adjusted on request. In our case we order a 5 μm crystalline Si device layer, a 1 μm SiO_2 buried thermal oxide and a 500 μm crystalline Si handle wafer. Use of SOI-type wafers for QUBIC is essential in order to control the deep etching of the substrate related to the manufacture of the suspended membranes. The recipe is adjusted for high etching selectivity

between Si and SiO_2, allowing to precisely remove the 500 µm handle-Si below the pixels. The SiO_2 acts as a barrier to stop etching and avoid removal of the remaining 5 µm Si device layer. On the top of this latter, an additional coating of 1 µm thick Silicon Nitride (SiN) is used to fabricate the suspended membranes. SiN membranes have very weak thermal conductivity at low temperature, being therefore well suited for low background CMB detector arrays. The SiN coating is realized by LPCVD (Low Pressure Chemical Vapor Deposition) in order to get reproducible super-low-stress layers, with tensile stress below 100 MPa. SOI substrates with coating on both sides are delivered by a Si-wafer manufacturer.

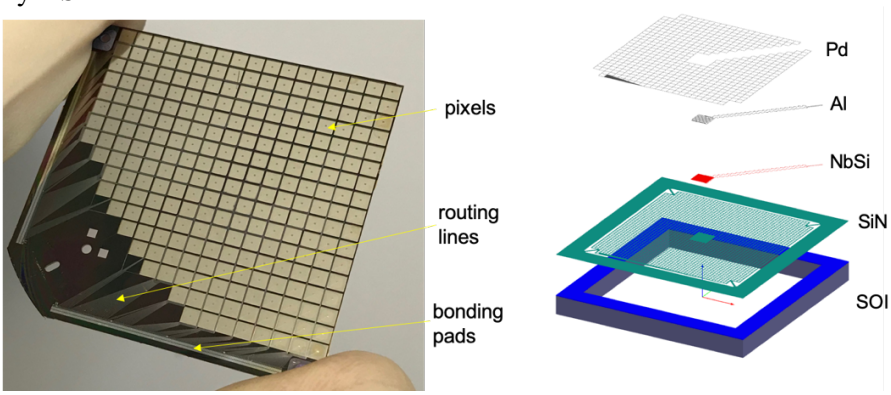

Fig. 1 *Left*, picture of a QUBIC 248-pixel TES array. *Right*, layout of the 3 mm pitch pixel structure. (Color figure online)

2.2 Routing and TES

The transition edge sensors, the routing lines and the bonding pads of the QUBIC arrays are realized in a common step based on the structuring of an evaporated bi-layer. This latter consists of 30 nm thick Nb_xSi_{1-x} deposited on the device-layer side of the SOI wafer, followed by 120 nm of Al. The bilayer is realized by e-beam co-evaporation of Nb and Si followed by e-beam evaporation of Al. It is important to keep the sample under vacuum between the two steps in order to avoid Nb_xSi_{1-x} oxide formation and get a high-quality proximity effect between the two layers. With the above-mentioned thicknesses, the bilayer behaves very similarly to pure Aluminum and is used for the routing and contact pads. Its transition temperature lies systematically between 1.1 and 1.2 K. The TES are made of pure Nb_xSi_{1-x}, by selectively removing the Al top-layer in the center of the pixels. We use a commercial Al wet etchant (MicroChemicals ANPE 80/5/5/10) that has a very high etching selectivity between Al and Nb_xSi_{1-x}.

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The Nb_xSi_{1-x} is an amorphous layer showing superconducting behavior for Nb concentrations *x* higher than 0.13. Its superconducting transition temperature (*Tc*) increases with Nb concentration and can thus be controlled upon our needs [6;7]. For the QUBIC 220 GHz focal plane, the concentration is adjusted to 0.155 ($Nb_{0.155}Si_{0.845}$) resulting to a *Tc* close to 500 mK (Fig 2). Homogeneity of the Nb_xSi_{1-x} composition along each wafer and reproducibility between wafers is crucial in order to get pixels with matched *Tc* and signal sensitivities.

Use of NbSi-Al bilayers suppress the problems of steps and contact impedance between the TES and the routing, simplifying considerably the lithography process. Due to the relatively high density of narrow lines (few microns), the routing step is the most demanding one in terms of lithography performance. Any defect at this stage can interrupt many routing lines reducing substantially the yield of operating-pixels. To avoid dust contamination, the routing is realized as a first step of our lithography process by lift-off. The SOI wafer is spin-coated with AZ5214 resist on its device-layer side. The routing patterns of the resist, after mask exposure and development, are observed under a microscope in order to operate a quality control and check if the yield of operating pixels is high enough (>90%) to proceed to the bilayer deposition. After lift-off of the NbSi-Al bilayer, the routing lines and the contact pads are visible. The TES appear during a second step dedicated to a selective Al wet etching. A patterned S1813 photoresist prevents Al etching of the routing and pads during this step.

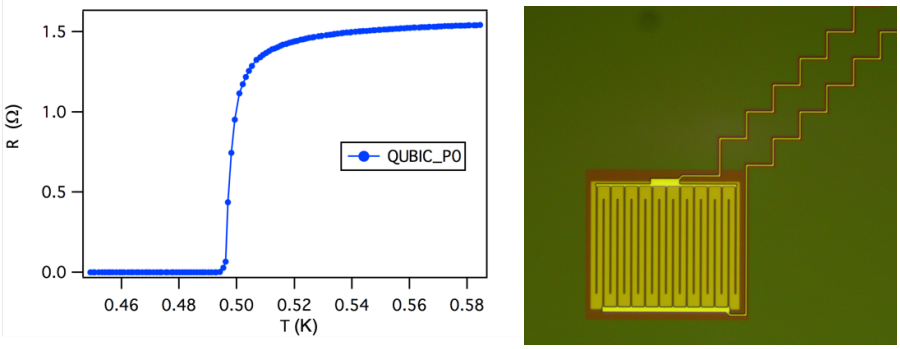

Fig. 2 *Left*, typical superconducting transition of a QUBIC $Nb_{0.155}Si_{0.845}$ TES. *Right*, optical photo of a TES with the comb electrodes and routing lines. The SiO coating protection of this structure is also visible. (Color figure online)

The square resistivity of a 30 nm $Nb_{0.155}Si_{0.845}$ film above its superconducting transition temperature is close to 600 Ohms, typically three orders of magnitude higher than usual TES. This is due to the fact that the Nb_xSi_{1-x} is a disordered amorphous alloy. In order to match to the noise of a SQUID amplifier, the normal state resistivity (R_n) of a TES must be of the

order of 1 Ohm or lower. To face this problem, the routing is extended on the top of our 240 x 280 μm^2 NbSi-TES in the form of a comb electrode structure (Fig. 2). This latter reduces the TES impedance by a factor of 400.

To avoid oxidation and damage from the etchants during the remaining steps of fabrication, the transition edge sensors and the routing lines are encapsulated with 25 nm of evaporated SiO. Coating of SiO can severely modify the stretch of our SiN membranes and must therefore be kept as thin as possible. Above 50 nm, deformation of the membranes is clearly visible and can result in a breakdown of the pixels. Lift-off lithography is used to delimit the SiO coating and keep the lateral pads free for the Al-wedge bonding of the array during its final integration to the SQUID readout.

2.3 Light absorption grid

Light absorption of the QUBIC arrays is based on a Pd grid placed at a $\lambda/4$ optical cavity resonator (λ being the photon wavelength). The grid design, realized by lift-off lithography, is adjusted to match the 377 Ohms square vacuum impedance in order to maximize light absorption efficiency. To obtain this, the grid filling factor if fixed to 10 % and Pd thickness to 10 nm. The structure is protected by a final 25 nm thick SiO coating. For 150 GHz photons the grid must be placed in front of a reflecting surface at a distance of 500 μm. The thickness of the SOI wafers is chosen to match this distance, the reflecting surface being the metallic back-holder of the arrays. At 220 GHz, the optimum thickness of the wafers is smaller.

2.4 Silicon deep etching

The remaining steps of the manufacturing process concerns the fabrication of the suspended membranes. The following three etching steps are realized: a deep reactive ion etching (deep-RIE) of the 500 μm handle-layer using the Bosch process, a RIE to structure the SiN membrane in a shape of a suspended grid and a dry etching of the 5 μm device-layer.

The Si deep-RIE is operated by repeated cycles of SF_6 plasma etching and C_4F_8 passivation with typical etching rates of 3 μm per minute. This process produces vertical wall etching independently of the Si crystalline orientation, allowing easy design of pixel cavities in the wafers. A 10 μm thick AZ4560 resist is applied on the back side (handle-layer) of the SOI substrate and mask-developed to a pattern of 3 mm pitch squares (2.7 mm size squares separated by 300 μm walls). The front side coatings are protected during this step with S1813 resist. The SOI is then mounted onto a 4 inches carrier Si-wafer using vacuum oil to ensure high thermal coupling and avoid overheating by the

plasma etching. The carrier wafer is cooled at 5°C during processing. The backside SiN coating and the SiO_2 buried oxide layers are respectively removed prior and after the 500 μm Si etching by switching the machine to a CHF_3 plasma recipe. The SOI is finally removed from the carrier wafer with care to avoid damage of the pixels and then cleaned with acetone and isopropanol. This Deep-RIE step is also used to cut the wafer to a square shape, allowing the assembly of four arrays on each focal plane.

2.5 Suspended SiN membranes

To realize the SiN suspended grid we use a CHF_3-CF_4 plasma RIE followed by a XeF_2 dry etching. Despite its fragility, the wafer is first spin-coated with S1818 resist, mask-exposed using the membrane grid pattern and developed into liquid AZ-developer. It then undergoes the RIE that shapes the SiN layer to a meshed membrane, standing on top of the 5 μm Si device SOI-layer. This latter is finally removed using XeF_2 dry etching. The existing S1818 resist is not dissolved prior to this etching in order to protect all previously deposited layers. XeF_2 gas allows homogenous attack of the device-layer without damaging of the SiN membranes. These last are finally released and must not be immersed into liquid anymore to avoid damage by capillary forces. The remaining resist on the top of the sample is removed by O_2 plasma etching and the array becomes available for low temperature calibration and integration into the QUBIC instrument. The measured Noise Equivalent Power (NEP) of these arrays is of the order of 5.10^{-17} W/sqrt(Hz) at 150 GHz and the membrane thermal decoupling is typically 100 pW/K for 500 mK TES [8].

3 Conclusion

The QUBIC instrument is based on an assembly of 248-pixel arrays whose manufacture is now well mastered. The pixels have a classical architecture of suspended meshed membranes for decoupling and NbSi TES that are thermally coupled to a grid for light absorption. Eight of these arrays will be integrated on the final QUBIC instrument to operate the 150 GHz and 220 GHz focal planes.

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